COLUMNAR FLOORPLAN

ABSTRACT OF THE DISCLOSURE

An FPGA is laid out as a plurality of repeatable tiles, wherein the tiles are disposed in columns that extend from one side of the die to another side of the die, and wherein each column includes tiles primarily of one type. Because substantially all die area of a column is due to tiles of a single type, the width of the tiles of each column can be optimized and is largely independent of the size of the other types of tiles on the die. The confines of each type of tile can therefore be set to match the size of the circuitry of the tile. Rather than providing a ring of input/output blocks (IOBs) around the die periphery, IOB tiles are disposed in columns only. Where more than two columns worth of IOBs is required, more than two columns of IOB tiles can be provided.